1st International Conference on
Microelectronics, Computing & Communication Systems
Advanced Regional Telecom Training Center

BSNL, Near Jumar River Bridge, Hazaribag Road, Ranchi-835217, Jharkhand, India
Tel: 0651-2273260, Mob. 9973886214, 8877101225
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INDIAN SOCIETY FOR VLSI EDUCATION

Dear Sir/Madam,

We are glad to inform you that ISVE Ranchi Centre is organizing two days 1st International Conference on **Microelectronics, Computing & Communication Systems (MCCS-2015)** with some other National & International Societies on 14-15th Nov-2015 at ARTTC, BSNL near Jumar River Bridge, Hazaribag Road, Ranchi.

Prospective authors are invited to submit full papers describing original, previously unpublished, complete work (not currently under review by another conference/ journal) up to six pages in IEEE double column format including figure, results and references. All papers send on conference e-mail: **mccs.2015.02@gmail.com, iete.isve.vlsi@gmail.com.** Papers will be accepted in word format only.

The accepted papers will be published in conference proceedings by Springer with ISBN number and extended versions of papers will be published in SCOPUS, SCI and some other indexed journals. (Name of Journals: 1-IETE Journal of Research (http://mc.manuscriptcentral.com/tijr), 2-IETE Technical Review, 3- JOLPE, 4-IETE Journal of Education, 5-WULFENIA, 6-TELEKOMANIKA,7-Analog Integrated Circuits and Signal Processing, 8- Microsystems Technologies(MST), 9- IJCA , 10- ARPN Journal etc).

MCCS-2015 will includes oral sessions and poster sessions, tutorials, invited talks, keynote address by renowned Scientists, Professors and Industry persons from India and Abroad on topics related to the conference. Original theoretical, practical, experimental, simulations, development, application, measurement, and testing based papers are invited for presentation in the conference. All submitted papers will go through rigorous plagiarism checking, language checking by expert's reviewers. Details review comments will be send to communicating authors in the form of Accepted, Accepted with changes, and Rejected.

Theme of the Conference:

International conference focused on the frontier issues in the Electrical, Electronics, Computer, Communication and Information Technology, Mechatronics, Environmental Science & Engineering, Bioengineering and their applications in business, academic, industry and other allied areas. This international

conference main aim to bring together scientists, researchers, engineers from academia and industry. It will provide an international forum to exchange and share their knowledge, experiences, technological developments, and researches in current trends.

Topics of Conference:

- Microelectronics, Circuit & Systems
- Nano-electronics Devices
- Micro Electro Mechanical System
- VLSI Design & IC Technology
- IC Fabrication and Testing
- VLSI Signal Processing
- VLSI for Wireless Communications
- VLSI for Bioengineering
- VLSI for Instrumentations & Controls
- VLSI for Electronic System Design & Manufacturing
- Image Processing
- Digital Signal Processing
- Embedded System
- Real Time Embedded System
- Robotics,
- Electric Power System
- Hybrid Vehicles
- Renewable Energy
- Green Energy
- Cloud Computing
- Algorithm development and implantation
- Computer Networks
- Computing systems
- Computer vision
- ICT Applications
- Computer Architecture
- Information Security, knowledge and data mining
- Software Engineering & Soft computing
- Image Sensing and Processing
- Parallel, grid and cloud computing
- Mobile Communication and Computing
- Ad hoc networks, Pervasive Computing
- Wireless Sensor Networks, Body Sensor Network,
- Sensor Network Applications in Mines,
- Antennae and Diversity
- EMI & EMC
- Satellite Communications
- Fibre Optics Communications and Optical Networks
- Quantum Dots
- Photonics & Optical Devices
- Bioengineering & Telemedicine
- RFID & Telemery Systems
- Envioronemtal Science & Engineering, Urban Planing
- Mechatronics
- Power Electronics

Books Publications on Pedagogy Methods:

Prospective authors are invited to submit full book chapters describing original, previously unpublished complete work (not currently under review by any conference/others) up to 30 pages including figures, tables and mathematical equations. Main heading font size should be: 16, subheading: 14 & normal texts: 12. All the contents will be accepted in **Time New Roman** only. All books will contain mission and vision. All book chapters will contain: (i) chapter overview, (ii) 5-7 chapter level objectives, (iii) 5-7 chapter units, (iv) 4-5 chapter level problems covering to all chapter objectives. Similarly each unit will contain: (i) 5-7 unit objectives, (ii) 4-5 unit level problems covering to all unit objectives, (iii) unit summary. For reference author can site Washington Acord. All book chapters send on conference e-mail: **mccs.2015.02@gmail.com,**

iete.isve.vlsi@gmail.com. Book chapters will be accepted in word format only. All submitted book chapters will go through rigorous plagiarism checking, language checking by expert's reviewers. Details review comments will be send to communicating authors in the form of accepted, accepted with changes, and rejected.

The accepted book chapters will be published by Springer / other reputed national/ international publishers with ISBN number/ ISSN number.

Name of Proposed Books	
• VLSI Signal Processing	• CMOS Digital VLSI Design with VHDL
• Microelectronics Devices & Circuits	• CMOS Digital VLSI Design with Verilog
• Advanced Semiconductor Devices & Photonics	• VLSI Communication Systems
• Environmental Science &Engineering	• Embedded System Design & Applications
• Fundamental of Electrical & Electronics Engineering	• Power Electronics & Control Systems
• Advanced VLSI Design with CADENCE	• Nano Science & Nano Technology

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About ARTTC Ranchi:- This is a Advanced Regional Telecom Training Centre of BSNL. It is 12 Km from Ranchi Railway station and 16 Km from Ranchi Airport**.** Ranchi is surrounded by hills, waterfalls, forests, and the other places of scenic beauty. Ranchi has a pleasant weather throughout the year. It is well connected by road, rail and air routes with all the major cities of India. The nearest airport and the railway station are in Ranchi. It has regular flight connectivity with New Delhi, Kolkata, Mumbai and Patna.

About ISVE: Indian Society for VLSI Education (ISVE) is registered (Act21, 1860) non profitable society dedicated to serve the nation. It makes a bridge between industry and academia for organizing the workshops, summer/winter schools, short term courses, conferences, symposiums and seminars by which students, research scholars, faculties and scientists come together, work together and share their knowledge in recent development in engineering, science & technology. Towards this end the society provides continuing

technical education programmes for human resource development. It is committed to innovative reseacrh, publications in recent trends in electrical, electronics, computers, communications, environmentals, biomedical & space engineering. The main aims of society to trend the manpower for **electronics system design and manufacturing** with the help of organizing the workshop, short term courses, symposium and conferences etc.

Registration:

1. Registration fee includes conference kit, breakfast, lunch, dinner and accommodation charges for two days.
2. Please download the **Registration Form** from the mail-attachment/website and send **scan copy of filled Registration Form** with **NEFT receipt** through **e-mail** for early registration. A/C Name: **INDIAN SOCIETY FOR VLSI EDUCATION**, A/C Number: **01670110061831**, IFSC Code: **UCBA0000167**,
   Bank: **UCO Bank**, Branch: **Mesra Ranchi**, Address: **BIT Main Building Mesra**, Dist: **Ranchi**, State: **Jharkhand**, Contact No: **0651-2275829**.

Categories of Delegates	**Before 30th Oct 2015 Indian Rs**	**After 30th Oct 2015 Indian Rs**	**Overseas USS**
Academia	10000/-	11100/-	1000
Students	8000/-	9000/-	900
Corporate Member	12000/-	13000/-	1200

3. 10% discount who will not be avail the accommodation & kit facility/ member of IEI/IEEE/IETE/ISVE/ISTE/IET/ACM. Please inform before the conference & send your membership proof with your form details.

Important Dates:

Important Points	**Previous date**	**Extended date**
Paper/ Book Chapter Submission Open	10th Aug 2015	10th Aug 2015
Paper/ Book Chapter Submission Deadline	30th Sept. 2015	30th Oct. 2015
Author Notification	15th Oct. 2015	5th Nov.2015
Last Date for Registration	30th Oct. 2015	10th Nov.2015
Camera Ready Paper/Book Chapters	30th Oct. 2015	10th Nov.2015
Date of Conference	14-15th Nov. 2015	14-15th Nov. 2015

Accommodation:

Accommodation**s** will be providing in **BSNL Guest House,** near Jumar River, Hazaribag Road, Ranchi and in some other Hotels in Ranchi for two days. Accommodation details will be communicated to the participants after his/her acceptance of papers and papers registration.

Sponsorship Opportunities:

We welcome sponsorship from companies and organizations who wish to show case their products and services and have the opportunities of networking with academics and practitioners in the field. With a truly global audience the conference provides an excellent opportunity for you to show your support for ongoing research and academic excellence by being involved with such important event. Academic institutions may choose to use sponsorship as a vehicle to promote their Masters and Ph.D. programmes. We also welcome sponsorship of specific activities in the conference programme. We believe that sponsoring a conference provides a superb vehicle to showcase your commitment to academic excellence and pursuit of knowledge. Your company will benefit from interaction with a highly focused, motivated, engaged and respective audience in a relaxed environment.

Sponsorship Type and Facility	**Diamond Rs. 1,00000/-**	**Platinum Rs. 70000/-**	**Gold Rs. 50000/-**	**Silver Rs. 20000/-**
Acknowledge at all events	Yes	Yes	Yes	
Complementary booth space	Yes	Yes	Yes	
List of sponsored displayed on conference webpage	Yes	Yes	Yes	Yes
Demo slot/Advertisement	20 Min	15 Min	10 Min	5 Min
Logo in proceeding and distributed to all authors	Yes	Yes	Yes	Yes
Memento & Standee Logo	Yes	Yes	Yes	Yes
Banner displayed during conference	12'x5'	8'x5'	6'x4'	3'x2'
Complementary conference Registrations with Kit	6	4	3	3

Organizing Secretary
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International Conference on Microelectronics, Computing & Communication Systems (MCCS-2015)
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		Pratim Kumar Saha[2], Abhijit Biswas[1], and Abhijit Mallik[3]	PERFORMANCE OF HYBRID CMOSFETS COMPRISING P-GE/ N-INGAAS MOSFETS WITH BARRIER LAYERS	
17	MCCS125	Monalisa Dutta[1], Soma Barman[2]	ELECTRICAL EQUIVALENT MODEL FOR GENE REGULATORY SYSTEM	38
18	MCCS129	Tara Prasanna Dash[1], Sanghamitra Das[2], Rajib K. Nanda[3], and C. K. Maiti[4]	DESIGN AND SIMULATION OF STRAINED-SI/SIGE CHANNEL P-MOSFETS	39
19	MCCS131	Sneha Jain[1], Vijaya Laxmi[2]	COLOUR IMAGE SEGMENTATION TECHNIQUES: A SURVEY	40
20	MCCS132	Parivesh Pandey[1], Vijaya Laxmi[2]	WIRELESS IMAGE SENSOR NETWORKS: A REVIEW	41
21	MCCS133	Suprojit Nandy[1], Soma Barman[2]	DESIGN OF A LOW COST HEART RATE MONITORING SYSTEM	42
22	MCCS134	A. Uma[1], T. Naveen Kumar[2], P.Kalpana[3]	DESIGN OF DA BASED FIR FILTER ARCHITECTURES USING LUT REDUCTION TECHNIQUES	43
23	MCCS135	K.Rajalakshmi[1], R.Nivedita[2]	FRACTIONAL DELAY FIR FILTER ARCHITECTURE USING NUMERIC STRENGTH REDUCTION TECHNIQUES	44
24	MCCS136	Yogesh Kumar Sharma[1], Sanjeet Kumar[2]	A CLUSTERHEAD SELECTION TECHNIQUE FOR A HETEROGENEOUS WSN AND ITS LIFETIME ENHANCEMENT USING HETEROLEACH PROTOCOL	45
25	MCCS139	N. Chattoraj[1], Abhijeet Pasumarthy[2], Rajeev Agarwal[3], Asifa Imam[4]	MODELING AND INVESTIGATION OF ELECTROTHERMALLY ACTUATED MICRO-GRIPPER	46
26	MCCS141	Pooshkar Rajiv[1], Rohit Raj[2], Ramakant Singh[3], Rishabh Nagarkar[4], Anurag Kumar Chaurasia[5], Sushant Agarwal[6], Vijay Nath[7]	AN ULTRA LOW POWER INTERNET CONTROLLED HOME AUTOMATION SYSTEM	47
27	MCCS142	Kamalini Devi[1], Jnana Ranjan Khuntia[2], Kishanjit Kumar Khatua[3]	DEPTH AVERAGED VELOCITY DISTRIBUTION FOR SYMMETRICAL AND ASYMMETRICAL COMPOUND CHANNELS	48
28	MCCS143	Bhabnai Shankar Das[1], Kishanjit K. Khatua[2], Kamalini Devi[3]	APPLICATION OF LATERAL DISTRIBUTION METHOD AND MODIFIED-LATERAL DISTRIBUTION METHOD TO COMPOUND CHANNEL HAVING CONVERGING FLOODPLAIN	49
29	MCCS151	Mohd.Javed Khan[1], Namrata Yadav[2], Jyoti Singh[3], Abhishek Pandey[4], Manish Kumar[5], Ashutosh Pranav[6], Madhu Kumari[7], Vijay Nath[8]	DESIGN OF CMOS INTEGRATOR CIRCUIT FOR SIGMA DELTA ADC	50
30	MCCS152	Namrata Yadav[1] ,	A 0.533 DB NOISE FIGURE & 7	51

		Mohd.Javed Khan[2], Jyoti Singh[3], Abhishek Pandey[4], Manish Kumar[5], Vijay Nath[6], L.K. Singh[7]	MILLWATT NARROWBAND LOW NOISE AMPLIFIER FOR GLOBAL POSITION SYSTEM APPLICATION	
31	MCCS181	Jyoti Singh[1], Megha Agarwal[2], Vinita Mardi[3], Madhu Ray[4], Deepak Prasad[5], Vijay Nath[6],Manish Mishra[7]	DESIGN OF ULTRA LOW POWER CMOS CLASS E POWER AMPLIFIER	52
32	MCCSB102	Shaligram Prajapat[1], Ram Jeevan Singh Thakur[2]	CRYPTIC MINING FOR AUTOMATIC VARIABLE KEY BASED CRYPTOSYSTEM	53
33	MCCSB105	Vidya T[1], N. Ramasubramaniam[2]	NOC DESIGN FOR INTERCONNECTING MULTI-CORES	54
34	MCCSB106	Shaligram Prajapat [1],Ram Jeevan Singh Thakur[2]	SOME RECENT DIRECTIONS TOWARDS DESIGN OF AVK BASED SYMMETRIC CRYPTOSYSTEM	55
35	MCCSB107	Tara Prasanna Dash[1], Rajib K. Nanda[2], Sanghamitra Das[3]	SILICON-GERMANIUM CHANNEL HETEROSTRUCTURE P-MOSFETS	56
36	MCCSB108	Abhishek Pandey[1], Suraj Kumar Saw[2], Jyoti Singh[3], Deepak Prasd[4],Vijay Nath[5]	DIGITAL IC DESIGN &TECHNOLOGY	57

MESSAGE

It gives me great pleasure to know that Indian Society for VLSI Education, Ranchi is organizing two days International Conference on Microelectronics, Computing & Communication Systems (MCCS-2015) on 14 - 15th Nov 2015.

Microelectronics technology has dramatically improved the capabilities of computers and communication systems, while also fueling the growth of completely new applications such as personal computers. Growing extremely fast and providing exceptionally powerful and inexpensive tools to manipulate electronic signals, microelectronics has become the cornerstone of information technologies. These computer and communications technologies are the basis for changes such as automation, energy conservation, and pollution control in offices, factories, automobiles, and homes; supercomputers for applications from weather prediction to computational research; new capabilities in financial services; advanced telephone and television systems; and complex weapons systems for national defense. Therefore, each of these areas is critically dependent on microelectronics technology.

The dramatic growth of technology has prompted observers to describe it as a micro-electronics revolution. Continuing to shrink the dimensions of electronic devices is important in order to further increase processor speed, reduce device switching energy, increase system functionality, and reduce manufacturing cost per bit. Approaches based on nano scale science, engineering and technology are expected to bring about a drastic change in the very nature of computing and communications.

I convey my best wishes for the success of the Conference and I am sure that it will bring together the brightest engineers and scientists from all over the world, through collaboration and exchange of ideas.

(Smriti Dagur)

Professor Anwr A. Khan
Ph.D., FIETE (India), SMIEEE (US A)
Former Professor of Physics &
Former *Vice Chancellor*
Ranchi University

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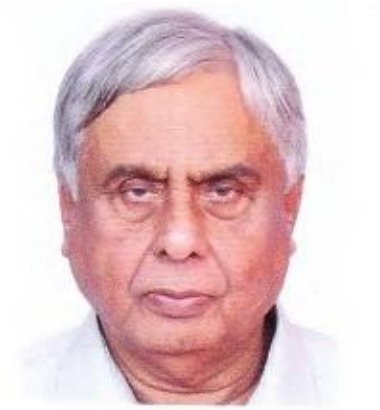

MESSAGE

I am happy to learn that Indian Society for VLSI Education, Ranchi, is organizing an International Conference on Microelectronics, Computing & Communication Systems (MCCS-2015) during November 14-15, 2015 at BSNL Advanced Regional Telecomm Centre, Hazaribag Road, Ranchi. The topic selected for the conference is of great global concern and its importance may be envisioned in the successful landing of Curiosity Rover on Mars in 2012. The Microelectronics has a much larger impact on world economy.

I am sure the different aspects of Microelectronic devices and their applications in Computing and Communication systems will be discussed in the conference and interaction of the young researchers with many distinguished experts in the field will make this Conference a grand success.

A. A. Khan

Anwar A. Khan

Pandey Vijay Bhushan Prasad
I.T.S.
Addl.G.M. (Mtce) ETR,
BSNL, Ranchi.

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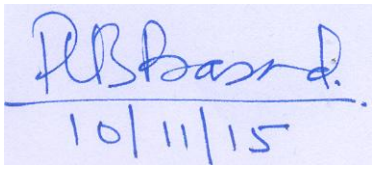
MESSAGE

It is my pleasure to welcome all of you to the 1st International Conference on Microelectronics, Computing & Communication Systems (MCCS-2015) with some other National & International Societies on 14-15thNov-2015 at ARTTC, BSNL near Jumar River Bridge, Hazaribag Road, Ranchi.

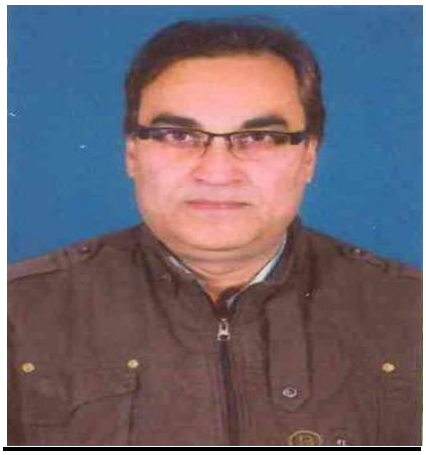
Advances in Microelectronics, Computing & Communication Systems and their technologies have led to many challenging problems that require new performance evaluation tools and methods to keep up with their rapid evolution and increasing complexity. This Conference is intended to provide an international forum for scientists, engineers, practitioners, network and communication users and students from Academia and Industry to share and exchange their experiences, discuss challenges, present original ideas, and report state-of-the-art and in-progress research results on all aspects of performance evaluation of Microelectronics, Computing & Communication Systems in the field of Electrical, Electronics, Computer, Communication and Information Technology, Mechatronics, Environmental Science & Engineering, Bioengineering and their applications in business, academic, industry and other allied areas .

This international Conference attracted research papers from various countries across the world, which were rigorously reviewed by the National & International Advisory Committee members and Subject Experts. I take this opportunity to thank them for their professionalism and valuable comments made to the authors. The accepted papers will be published in conference proceedings by Springer with ISBN number and extended versions of papers will be published in SCOPUS, SCI and some other indexed journals.

Many people have kindly helped us to prepare and organize the MCCS-2015 Conference. First of all, I would like to thank Chairman Committee, Co-chairman Committee, Organizing Secretary, General Chair, International Advisory Committee, National Advisory Committee, Technical Programme Committee, Joint Secretary for their support, guidance, and help for making the Conference a successful event. Also, I would like to give my special thanks to all who helped and contributed to the success of this Conference. Finally, I would also like to thank all the authors and participants for selecting the MCCS-2015 Conference to submit their contribution.



(Pandey Vijay Bhushan Prasad)
Chairman ISVE



MESSAGE

I come to know that **Indian Society for VLSI Education, Ranchi** is organizing two days International Conference on Microelectronics, Computing and Communication Systems (MCCS-2015) on 14th -15th November, 2015 at ARTTC, Ranchi. I appreciate the theme of this event and participation of the delegates. I think that outcomes of this conference will add in the development of our country.

I congratulate the members of organizing committee for their effort in the organization of the event and wish a great success of the conference.

Shree Sanjay Kumar Jha
Chiarman, IETE, Ranchi Centre.

INDIAN SOCIETY FOR VLSI EDUCATION
RANCHI

MESSAGE

It is eminence pleasure for us that **Indian Society for VLSI Education (ISVE) Ranchi** centre gives me the opportunity for General Chair in two days 1st International conference on Microelectronics Computing and Communication Systems (MCCS-2015) organised at Advanced Regional Telecom Training Centre BSNL near Jumar River Hazaribag Road Ranchi on 14th -15th November -2015. Really this conference will provide the international forum to exchange research idea in the area of VLSI Design, Micro/Nanoelectronics, Circuits, Computing, Communication Systems, Analog and Digital Signal Processing, Embedded System Design, Green Energy, Smart Power Plants, Aerospace Application, Biomedical Instrumentation and Engineering, Civil and Environmental Science, E-governance, etc. I hope this conference will give the platform for the researchers to exchange their ideas and publish his article in highly reputed publications. The main focus of this conference is to enhance the feasibility of electronic system design and manufacturing in the country. As everybody know my Country is good consumers of electronics goods, but production is approx 5 to 10% of total consumptions. This conference will provide the guidance by expert researchers how to develop electronic goods in enough amounts in the country. On behalf of the general chair I welcome to all the participants, expert speakers, session chairs, international and national advisory board members, technical program committee members, expert reviewers, technical and nontechnical persons, media persons, intellectual persons of India and abroad for his/her constant support and inspiration for conducting this conference successfully. These societies are continuously support to government activity to trend the engineers, researchers, professors by organising conference, symposium, workshop, short term courses, summer and winter schools in VLSI design for **electronic system design and manufacturing(ESDM)**. Once again I heartily welcome to all associated members from district, state, country and abroad who are directly and indirectly supporting to this conference for grand success.

Dr. Vijay Nath
General Chair_MCCS-2015

INDIAN SOCIETY FOR VLSI EDUCATION
RANCHI

MESSAGE

It is a matter of extreme pleasure that **Indian Society for VLSI Education, Ranchi** is organizing two days 1st International Conference on **Microelectronics, Computing and Communication Systems (MCCS-2015)** on 14th -15th November, 2015 at ARTTC, Ranchi. The "Digital India" and "Skilled India" are the vision of our Hon'ble Prime Minister Sri Narendra Modi. So, the theme and sub-themes of this conference is designed to come out with the authentic research works in the field of Electronics and Telecommunication.

I welcome all delegates from International arena as well as the different corners of the country for their active participation in the conference. I also appreciate the executive capacity of Dr. Vijay Nath and all the best to the members of the organizing committee.

Dr. Anand Kumar Thakur.
Organizing Secretary_MCCS-2015
Hony. Secretary, IETE, Ranchi Centre

University of Kalyani

FACULTY OF ENGINEERING, TECHNOLOGY & MANAGEMENT

Prof. J. K. Mandal
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MESSAGE

I am glad to learn that **Indian Society for VLSI Education, Ranchi** is organizing two days International Conference on Microelectronics, Computing & Communication Systems (MCCS-2015)on 14th and 15th, November 2015 at Advanced Regional Telecom Centre, BSNL Hazaribag Road Ranchi-835217 Ranchi

I am also happy to know that the accepted papers will be published by a reputed publisher with ISBN number and extended version of selected papers will also be published in journals of good reputation and indexing.

This will be a very good platform to share the current trend of technology among researchers, scholars and industry people.

My best wishes for MCCS 2015.

Prof.(DR.) J. K. Mandal
Professor & Former Dean, FETM
Kalyani University

List of Messages of Eminent Persons

Message of President IETE New Delhi	Smt. Smiriti Dagur, New Delhi
Message of Former Vice Chancellor, RU	Dr. A.A. Khan,
Message of TPPC IETE	Dr. A. K. Saini
Message of Guest of Honor	Sh. Sanjay Kumar Jha, Chairman, IETE Ranchi
Message of Keynote Speaker	Dr. Abhijit Biswas, University of Calcutta
Message of Invited speakers / Keynote speakers	Dr. P.K. Barhai, Former VC BIT Mesra
Message of Expert Invited Lecture	Dr. J.S. Roy, KIIT Bhubneshwar
Message of Expert Invited Lecture	Dr. J.K. Mandal, Kalyani University
Message of Expert Invited Lecture	Dr. S.P. Tiwari, IIT Jodhpur
Message of Expert Invited Lecture	Dr. Manish Mishra, DDU University Gorakhpur
Message of Chairman IVSE, Ranchi	Sh. Pandey Vijay Bhushan Prasad, DGM ETR, BSNL Ranchi
Message of Co-chairman MCCS-2015	Sh. Ranjan Kumar Ram , DE(TX) BSNL Ranchi
Message of General Chair MCCS 2015	Dr. Vijay Nath, BIT Mesra, Ranchi
Message of Organizing Secretary MCCS 2015	Dr. Anand Kr. Thakur SSMC, RU
Message of expert Invited Lecture	Dr. K. Solomon Raju, CEERI Pilani
Message of expert Invited Lecture	Dr. K. Khatua, NIT Rourkela

List of Session Chair Persons

S.N.	Name of Chair Persons	Institute/ University
1	Dr. A. A. Khan	Ranchi University
2	Dr. Abhijit Biswas	University of Calcutta
3	Dr. P.K. Barahi	Former VC BIT Mesra
4	Dr. J.K. Mandal	Kalyani University
5	Dr. J.S. Roy	KIIT Bhubaneswar
6	Dr. S.P. Tiwari	IIT Jodhpur
7	Dr. K. Khatua	NIT Rourkela
8	Dr. Mahesh Chandra	BIT Mesra
9	Dr. P.R. Thakura	BIT Mesra
10	Dr. R.K. Lal	BIT Mesra
11	Dr. S.S.Tripathi	BIT Mesra
12	Dr. K.K. Senapati	BIT Mesra
13	Dr. V.K. Jha	BIT Mesra
14	Dr. Vijay Nath	BIT Mesra
15	Dr. Anand K. Thakur	SSMC RU
16	Dr. I. Mukherjee	BIT Mesra
17	Dr. A. Islam	BIT Mesra
18	Dr. Dileep Kr. Upadhyay	BIT Mesra
19	Dr. K. Solomon Raju	CEERI Pilani
20	Dr. Manish Mishra	DDU GU
21	Dr. Gaurav Trivedi	IIT Guwahati
22	Dr. P. Kumar	IIT Patna
23	Prof. Richa Pandey	BIT Mesra
24	Dr. Umesh Yadav	DDU GU
25	Dr. Vijay Laxmi	BIT Mesra
26	Dr. A.K. Tiwari	BIT Mesra
27	Dr. N. Chattoraj	BIT Mesra
28	Dr. Sukalayan Chakraborty	BIT Mesra
29	Dr. Rajeev Agarwal	BIT Mesra

30	**Dr. D. Devraj**	**KLU Tamilnadu**
31	**Dr. Manish Mishra**	**DDU GU**
32	**Dr. S.S. Sahu**	**BIT Mesra**
33	**Dr. Sanjeet Kumar**	**BIT Mesra**
34	**Sh. Vijay Bhusan Pandey**	**ARTTC, BSNL Ranchi**
35	**Sh. Ajay Kumar**	**ARTTC, BSNL Ranchi**
36	**Dr. S. K. Mahapatra**	**BIT Mesra**
37	**Dr. R. K. Sinha**	**BIT Mesra**
38	**Dr. Soma Berman**	**University of Calcutta**
39	**Prof. D. Acharjee**	**ISTM Kolkata**
40	**Prof. Shahiruddin**	**BIT Mesra, Patna Campus**
41.	**Dr. Vinay Gupta**	**Delhi University**

INDIAN SOCIETY FOR VLSI EDUCATION
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MCCS104

SINGLE MODE NEGATIVE DISPERSION HEXAGONAL PHOTONIC CRYSTAL FIBER

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[2] Dept of ECE, National Institute of Technology, Patna, India

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***Abstract*—A Photonic Crystal Fiber (PCF) with circular air holes having low dispersion and low confinement loss is analyzed. By deliberate selection of dimensions of air holes and spacing between air holes it is possible to obtain the two required properties of solid core PCF at wide wavelength range that is negative dispersion and low confinement loss which is of the order of 10^{-7} dB/m. At 1.55μm wavelength with common pitch (Λ) the simulated results has been observed at different diameter. The intended design finds applications in communication fields.**

***Keywords*— Air Fill Fraction, Confinement Loss, Dispersion, Finite Element Method, Photonic Crystal Fiber.**

INDIAN SOCIETY FOR VLSI EDUCATION
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MCCS105

A SECURE THREE-FACTOR REMOTE USER AUTHENTICATION SCHEME USING ELLIPTIC CURVE CRYPTOSYSTEM

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***Abstract*— Recently, three-factor such as biometric, smart card and password based authentication schemes have drawn considerable attention in the field of information security. In this paper, the authors have presented an Elliptic Curve Cryptosystem based authentication scheme using biometric, smart card and password and also analyzed the formal and informal security of the authentication scheme. In this scheme, the parameters of elliptic curve are derived from the biometric features like iris, fingerprints etc. which is suitable to withstand the forgery. The formal and informal security analyses are done based on the BAN logic and suggested preposition respectively. The security analysis ensures that the presented scheme can withstand various kinds of malicious attacks. In addition, the scheme is also comparable with other related scheme in the context of communication cost, computation cost and smart card storage. The scheme is suitable to ensure high degree of security with reduced comparatively overhead.**

***Keywords*— Authentication; BAN logic;Biometric; Key Agreement; Elliptic Curve Cryptography (ECC);Smart card**

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MCCS106

IMPLEMENTATION OF FINGERPRINT-BASED BIOMETRIC SYSTEM AND ITS INTEGRATION WITH HRMS APPLICATION AT RDCIS, SAIL

S Selvi[1], Manas Rath[2], N N J Hemrom[3], A Bhattacharya[4], A K Biswal[5]

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Abstract: **RDCIS is a R&D unit of Steel Authority of India Limited (SAIL). RDCIS has implemented Human Resource Management System for management of online leave applications, tour applications, dependant declaration, medical validation of employees etc. for quickly building the workflows and processes of HR functions. At RDCIS, there are around 481 employees and 223 Contract Workers working under different Contractors. RDCIS main office is located at Ranchi, RDCIS Plant Centre's are located at Bhilai, Bokaro, Rourkela, Burnpur, Durgapur and Bhadravati. SAIL has its own network connecting all the Steel Plants and City offices. RDCIS has own VLAN network and connected to RDCIS Plant Centre's through SAIL-Net. Before the implementation of biometric system, the employee attendance was captured in the attendance register. Attendance from plant centre's and city offices was sent through e-mail system every month to RDCIS, Ranchi.**

Keywords: **HRMS - Human Resource Management System, MIS - Management Information System, C&IT - Computer & Information Technology, RDCIS - Research and Development Centre for Iron & Steel, SAIL - Steel Authority of India Limited, HR – Human Resource, P&A – Personnel & Administration, JSP – Java Server Pages, GM – General Manager, HoG – Head of Group.**

INDIAN SOCIETY FOR VLSI EDUCATION
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MCCS110

DESIGN AND FPGA IMPLEMENTATION OF EFFICIENT CORDIC BASED 2D-DCT USING HDL

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Abstract: **In this Paper, novel idea behind the CORDIC algorithm used for recent DSP application is due to very attractive and easy method. Using this method, it has not only reduces the complexity in the computation of 2D –DCT but also reduces the latency and increases throughput output like parameters. This paper has introduced a Field Programmable Gate Array (FPGA) implementation of a CORDIC processor that provides high performance and an efficient implementation area. For the fast computation in DCT processor have tried to avoid multiplication operations by increasing number of shift and addition operations by using a CORDIC algorithm which reduces the complexity in a computation.. The 1D- DCT is useful in processing one-dimensional signals such as speech waveforms. For signal processing of images, we need a two dimensional (2D) version of the DCT data, especially in coding for compression techniques, for its optimistic performance. This paper has presents the FPGA implementation of CORDIC algorithm for 111.048 MHz frequency 2D-DCT using HDL simulation with the help of Xilinx 14.7.**

***Keywords*—1D-DCT, 2D-DCT, Discrete Cosine transform, CORDIC.**

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MCCS111

FABRICATION AND INVESTIGATION OF LOW VOLTAGE PROGRAMMABLE FLASH MEMORY GATE STACK

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Abstract- **In this paper, fabrication, characterization and analysis of a FGMOS gate stack employing ultra-thin tunnel oxide of 3 nm thickness is discussed. Apart from basic C-V and G-V profiles, high frequency hysteresis curve has been investigated and device level parameters are extracted. Use of ultra-thin tunnel oxide has facilitated direct tunneling mechanism at program/erase voltages of 10 V for 200 ms and -8 V for 40 ms, respectively. Excellent memory window of 1.2 V has been obtained. Frequency dependent capacitance and reliability related profiles are also studied. The device is useful for power efficient non-real-time applications like data logging, biometric security, back-up servers etc.**

Keywords:- **FGMOS gate, memory window.**

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MCCS112

AN EFFECTIVE METHOD FOR MAINTENANCE SCHEDULING OF VEHICLES USING NEURAL NETWORK

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Abstract: **The maintenance scheduling of vehicles of a transportation system has its own significance as far as effective operation of a transportation system is concerned. Presently, inspection planning is used to plan for maintenance activity of vehicles in a transportation system. It helps the operator to organize maintenance activity and increase the ability to identify a proactive failure situation. In order to avoid the dilemma like premature aging and failure of vehicles in transportation system responsible for spontaneous and costly maintenance charges, at regular intervals it is imperative to carry out preventive maintenance (PM). This paper presents the application of neural network technique for automatic maintenance scheduling of vehicles. This paper presents an economic method for solving maintenance scheduling of medium type vehicles by exploiting the neural network technique.**

Keywords- **Maintenance scheduling, Preventive maintenance, Neural network.**

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MCCS114

IMPROVED CLUSTERING FOR CATEGORICAL DATA WITH GENETIC ALGORITHM

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***Abstract*-Clustering is the most significant unsupervised learning, in which the aim is to partition a given set of data elements into homogeneous groups called clusters. However, working only on numeric values limits its use in data mining because data sets in real world often contain categorical values. The *k*-modes algorithm is one of the very effective for proper partitions of categorical datasets, though the algorithm stops at locally optimum solution as depended on initial cluster centres. Proposed algorithm utilizes the genetic algorithm (GA) to optimize the *k*-modes clustering, because considering noise as cluster centres gives the high cost which will not fit for the next iteration also avoids major limitation of getting stuck at locally optimal values. Its superiority over popular categorical clustering algorithms and other genetic algorithm-based clustering method, is extensively demonstrated for several artificial and real life data sets. Moreover, the accuracy is increased proves method is efficient and can reveal encouraging results especially for the large datasets.**

Keywords: Clustering; Categorical data; genetic algorithm; k-modes algorithm.

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MCCS115

AN ADAPTIVE APPROACH OF BIOMETRIC BASED AUTHENTICATION IN ATM USING DEEP LEARNING

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***Abstract*—Biometric based authentication in ATM is all concerning preventing dishonest activities and to conjointly produce a lot of security in authentication, to the prevailing system by the utilization of iris recognition. With this system, eye image of a private user is captured at the dealing terminal from that the iris is extracted from the image by Canny's edge detection and Hough's algorithmic program. Once a dishonest dealing is committed, enforcement officers will use the iris featured for the dishonest person which can be compared (Aadhar card) Government database details to catch criminals. Iris recognition is an automatic methodology of identifying and verification that uses mathematical pattern-recognition techniques on video pictures of a human eye, whose complicated random patterns, unique and can be seen from some distance.**

A key advantage of iris recognition, besides its speed of matching and its extreme resistance to False Matches is the stability of the iris as an internal, protected, yet externally visible organ of the eye. Deep learning is currently an extremely active research area in machine learning and pattern recognition society.

***Keywords*—Iris recognition, Houghs algorithm, canny edge detection, security in ATM's, Feature Representation, Neural Networks, Deep Learning, GPGPU Optical Character Recognition and Machine Learning separated by commas**

INDIAN SOCIETY FOR VLSI EDUCATION
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MCCS116

UNIVERSALLY VERIFIABLE CERTIFICATELESS SIGNCRYPTION SCHEME FOR MANET

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***Abstract*— The mobile ad-hoc network (MANET) is a collection of wireless mobile nodes that communicate with one another through a standard transmission medium such as, Wi-Fi, cellular or satellite communication. However, their basic characteristics make them vulnerable against numerous attacks accordingly raising the need of security. In this paper, we propose a certificateless signcryption scheme based on the difficulty of solving the Diffie-Hellman problem. The simulation result proves that the scheme is secure against active and passive attacks using AVISPA (Automated Validation of Internet Security Protocols and Applications) tool.**

***Keywords*—mobile ad-hoc network; certificateless signcryption; AVISPA Tool.**

INDIAN SOCIETY FOR VLSI EDUCATION
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MCCS118

IMPACT OF SIDEWALL SPACER LAYERS ON THE ANALOG/RF PERFORMANCE OF NANOSCALE DOUBLE-GATE JUNCTIONLESS TRANSISTORS

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***Abstract*- Using extensive numerical device simulation we investigate the influence of sidewall spacers on the analog/RF performance of double gate junctionless transistors at channel length of 30 nm. Our findings reveal that peak transconductance and peak intrinsic gain increase by 5.2 % and 71.3 % for spacer dielectric constant k = 30 as compared to the respective values for k = 3.9 while peak unity gain cut-off frequency increases by 37 % for k = 3.9 compared with the value for k = 30. The transconductance generation factor is found to be less sensitive to the variation in k. With increasing k the output conductance becomes less for low gate overdrive voltage VGT while it shows a reverse trend for higher VGT. It is evident from our studies that peak transconductance, peak transconductance generation factor, peak gain and peak cut-off frequency increase by 13 %, 10 %, 27 % and 20 %, respectively, for spacer length of 5 nm compared with the corresponding values for spacer length of 15 nm. However, with a larger spacer length the output conductance exhibits reduced value for lower VGT, while it becomes comparable with the values for smaller spacer lengths as VGT increases.**

***Keywords*- Analog /RF performance, Double-gate MOSFET, gain, junctionless transistor, spacer layer, unity-gain cut-off frequency.**

INDIAN SOCIETY FOR VLSI EDUCATION
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MCCS119

A NOVEL DATA ENCRYPTION APPROACH IN THE GRID STRUCTURED BINARY IMAGE

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Abstract: **Data hiding from external malicious access is an important and timely issue. Cryptography is the back bone of information or processed data security. The existing cryptography techniques provide good security, however its computational complexity is also very high. Hence, there is a need of an efficient as well simple cryptography approach. In this context, the paper proposes a novel technique for cryptography in the form of binary textures. The binary textures provide a form of security corresponding to the original message. The binary textures are generated, reshuffled and arranged in an image form to make it robust from malicious access. The reliability of the proposed approach has been illustrated with some empirical case studies. The overall cryptography process in a digital image makes it a simple, low cost and effective methodology for the secure communication.**

Index terms- **Grid Structured, Cryptography, Binary Image, Texture, Shuffling pattern**

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MCCS120

BALANCED WRAPPER DESIGN TO TEST THE EMBEDDED CORE PARTITIONED INTO MULTIPLE LAYER FOR 3D SOC TARGETING POWER AND NUMBER OF TSVS

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Abstract- **With the advancements in fabrication technology, the manufacturing of three dimensional (3D) IC chips is now feasible. However, design and testing tools in this regard are still not mature. One of the main challenges is to reduce the total time for testing of such chips. In order to reduce the test application time, the wrapper design must be balanced such that all scan chain lengths are almost of equal length. This work minimizes the scan test time with the available number of through silicon vias (TSVs). The Verilog coding for the proposed implementation has been done using Cadence tool to analyze power and delay.**

Keywords **– Scan chain, wrapper, 3D IC, test access mechanism, TSV**

INDIAN SOCIETY FOR VLSI EDUCATION
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MCCS121

Analysis of Electromagnetic Wave Using Explicit FDTD in TM Mode with Extrapolation

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Abstract- **In this paper, an Explicit Finite Difference Time Domain (FDTD) method is used for Electromagnetic wave analysis. Explicit method has computational simplicity in linear medium with superior stability by the CFL condition. The method is unstable with non-linear mediums when materials have $\varepsilon_r > 1$. Here a conventional Explicit FDTD method is used along with Interpolation and Extrapolation technique for the EM wave analysis in TMz mode. Deriving the higher order approximations from a lower order approximation is called as Extrapolation. This technique is used to eliminate the second order error $O(h^2)$ terms from first order central difference approximation. The propagating wave Ez in TM mode is the summation of two triangular waves of Hx, Hy fields, which in turn form a five point wave stencil. The wave propagates through the grid using a cell centered technique. The propagation speed of the wave depends on necessary parameters such as numerical dispersion of grid, time-step (Δt), x and y spatial step (Δx) and (Δy).**

Keywords**—Finite Difference Time Domain(FDTD); CFL; ElectroMagnetic(EM); Central Difference Time Domain(CDTD); Explicit; Transverse Magnetic(TM); Interpolation; Extrapolation.**

INDIAN SOCIETY FOR VLSI EDUCATION
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MCCS122

A HOLISTIC APPROACH FOR HARMONIC ELIMINATION IN SINGLE PHASE GRID CONNECTED PHOTOVOLTAIC SYSTEM

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***Abstract*—Photovoltaic system is one of the renewable sources of energy utilized with conventional systems to meet the increasing power demand. The topology considered is a single-phase grid connected photovoltaic (PV) system in which the inverter unit plays an important role. Harmonic currents injected into the grid by PV inverters will downgrade the power quality of the grid and causes an increase in the total harmonic distortion (THD) at the output of the inverter. This paper focus on the current control strategy adopted by the inverters for harmonic elimination and hence for the reduction of THD for ensuring high quality of the current injected into the grid. A current based maximum power point tracking (CMPPT) method is implemented for a single phase photovoltaic power conditioning system. The current based MPPT method makes the entire control structure of the power conditioning system simple and uses an inherent current source characteristic of solar cell array. The conventional Proportional - Integral (PI) controller is replaced with PR controller in this system. In this work a proportional-resonant-integral(PRI) controller and its design is proposed to achieve unity power factor operation as well as better harmonic elimination.**

***Keywords*—photovoltaic(PV); total harmonic distortion (THD); proportional resonant integral (PRI) control; adaptive harmonic compensation; Genetic Algorithm (GA).**

INDIAN SOCIETY FOR VLSI EDUCATION
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MCCS123

A DEA BASED EVOLUTIONARY COMPUTATION MODEL FOR STOCK MARKET FORECASTING

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***Abstract*—Stock market forecasting is used to draw attention of researcher since long and it will be. In this paper a Data Envelop Analysis based Gene Expression Programming model has been proposed and experimented with real data from BSE Sensex. The DEA has been used for filtering independent variables to be used as input variable of the GEP model. Different experiments has been made by first al-lowing all input variables to the GEP model directly without filtration by DEA and then allowing only those variables which are tested and marked as better variable to explain target variable. The result obtained from both the experiment has been put side by side and explained. From the analysis it was noticed that the DEA based GEP has better capabilities to forecast than the other one, even with less number of input variables.**

***Keywords*—Data Envelop Analysis, Gene Expression Programming, Stock Market forecasting**

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MCCS124

INVESTIGATIONS ON THE LOGIC PERFORMANCE OF HYBRID CMOSFETS COMPRISING P-GE/ N-INGAAS MOSFETS WITH BARRIER LAYERS

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***Abstract*—We investigate the logic performance of hybrid CMOS devices comprising Ge channel pMOSFETs and InGaAs channel nMOSFETs with Si and InP barrier layers, respectively, at channel length L_g = 20 nm and 30 nm. The performance has been evaluated in terms of rise time, fall time, noise margin of hybrid CMOS inverters, and frequency of oscillations and energy-delay product of ring oscillators built using hybrid CMOS devices. Our findings show that the rise time and fall time of hybrid CMOS inverter reduce by 92.16% and 82.47%, respectively, as compared to the corresponding values for Si CMOS at L_g = 30 nm. The static noise margin for hybrid CMOS inverters improves 80.11% compared to Si values at L_g= 30 nm. Oscillation frequency of a 3-stage ring oscillator is found to be 263.94% higher when compared with its Si counterpart. Also there is an improvement of 17.79% and 77.38% in power-delay and energy-delay product, respectively, for hybrid CMOS inverters in comparison with their equivalent Si counterparts for a channel length of 30 nm. Similar trend is observed for channel length of 20 nm.**

***Keywords*—Hybrid CMOS, logic performance, power-delay product, noise margin, rise time, fall time, frequency of oscillations.**

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MCCS125

ELECTRICAL EQUIVALENT MODEL FOR GENE REGULATORY SYSTEM

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***Abstract*— An electrical network model is designed to represents the central dogma of molecular biology and simulate the response to study the behaviors of bacteria gene E.Coli. The transcription, translations processes of biological system is represented by differential equations. These equations are mapped into electrical domain and a equivalent electrical circuit is realized. The electrical response of circuit is simulated in Spice domain and result shows the structural and repressor protein behaves like a toggle switch which truly match with biological system.**

***Keywords*—Operon; genetic switch; electrical model; gene regulation; central dogma; ordinary differential equation(ODE).**

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MCCS129

DESIGN AND SIMULATION OF STRAINED-SI/SIGE CHANNEL P-MOSFETS

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Abstract—Device simulations have been applied to study the performance enhancements of strained-Si/SiGe channel heterostructure MOSFETs. The effects of low temperature operation on the performance of MOSFETs have also been studied and discussed in terms of threshold and output characteristics.

***Keywords*—Heterostructure MOSFET, hetero-FET, device simulation.**

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MCCS131

COLOUR IMAGE SEGMENTATION TECHNIQUES: A SURVEY

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Abstract- **In today's world, where digital image processing is becoming an essential part of technology, segmentation of images poses a challenging problem. Before any complex task to be done on images, segmentation is a prerequisite. Segmentation ensures the simplification of a problem by changing the representation of an image from a complex one to a more analytical and easier form. Pixels of segmented regions share common characteristics. Perfect segmentation is difficult to obtain. There exist many techniques which have been applied such as, edge based segmentation, region based segmentation, morphological operations, thresholding, clustering methods, etc. Segmentation has a crucial role in image analysis. The accuracy of segmentation determines the success or failure of computer algorithms. Therefore, there is a need to develop efficient and less time consuming algorithms for segmentation. This paper summarizes a number of segmentation methods.**

Index terms- **Clustering, Edge Maximization Technique, Segmentation, Thresholding, Watershed algorithm.**

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MCCS132

WIRELESS IMAGE SENSOR NETWORKS: A REVIEW

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Abstract- **Wireless Sensor Networks were extensively used in monitoring and observing a particular region. WSN combination of nodes and can be sensitive to pressure, temperature, motion, sound etc. This paper represents the survey of design and implementation of Wireless Image Sensor Network, which is an integral part of monitoring and surveying the subjective region visually. Image sensor nodes are accoutred with miniature visual camera and RF module for communication. The camera node provides visual information and then transmitted to another node wirelessly using ZigBee. Several challenges in sensor networks are discussed that can enhance performance and efficiency of modern day sensor networks, As it turns out FPGA can reduce computational cost through on-board image processing. We discuss that combination of micro-controllers and FPGA can play a major role in future, in areas where processing capabilities such as compression, cryptography and transmission of data are important.**

Keywords- **ZigBee, FPGA**

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MCCS133

DESIGN OF A LOW COST HEART RATE MONITORING SYSTEM

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***Abstract*—With the development of health consciousness and growing of aging population, home based health monitoring has become a key research area for information and communication technology. The objective of the paper is to monitor heart rate of a person in a low cost and reliable way. The system is implemented in Labview environment.**

***Keywords*— Piezoelectric sensors; Heart rate; Micro-controller; ECG; Filters.**

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MCCS134

DESIGN OF DA BASED FIR FILTER ARCHITECTURES USING LUT REDUCTION TECHNIQUES

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***Abstract*— The Multiplier-less techniques such as Distributed Arithmetic (DA) has gained large popularity for its high speed processing. Architectures based on DA results in cost efficient and area efficient structures. This paper presents design and realization of various DA based FIR filter architectures based on LUT reduction techniques of length N=4 and also implemented using both shift accumulators and Carry save shift accumulators. The larger LUT is sub divided into a number of LUTs to reduce the size of the LUT for higher order filter.FIR filter architectures designed include filter with LUT size of 2^N-1 words, filter with LUT size of 2^{N-1} words, filter with LUT breakup contains two $2^{N/2}$-1 word LUTs, and also LUT-less filter but only has combinational blocks. These filter architectures have been synthesized for the target FPGA device and results are compared based on RTL area, device utilization, maximum operating frequency and power consumption.**

***Keywords*—Distributed arithmetic (DA), Carry save shift accumulator (CSSA), Shift Accumulation (SA).**

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MCCS135

VLSI IMPLEMENTATION OF SMITH-WATERMAN ALGORITHM FOR BIOLOGICAL SEQUENCE SCANNING

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***Abstract*—This paper presents the design and implementation of Smith-Waterman algorithm. The aim of this work is to improve the speed of the algorithm by applying optimization concepts of VLSI signal processing such as retiming and parallelism. This facilitates the reduction of critical path and computational time of the algorithm. The algorithm is implemented in Simulink - MATLAB 2013 and the corresponding Verilog codes are written and synthesized in Xilinx ISE Design Suite 14.7.**

***Keywords*—Smith Waterman algorithm, bio sequence, VLSI signal processing.**

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MCCS136

A CLUSTERHEAD SELECTION TECHNIQUE FOR A HETEROGENEOUS WSN AND ITS LIFETIME ENHANCEMENT USING HETEROLEACH PROTOCOL

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***Abstract*—WSN consists of hundreds or even thousands of nodes, which increases the reliability of the data but at the same time it also increases the redundancy of the collected data. So, the role of cluster head is important to reduce the redundancy generated in a sensor network, since early die out of cluster head may result in network breakdown or lifetime reduction of a WSN. This paper proposes modified LEACH algorithm in heterogeneous network named as HETEROLEACH. It increases the lifetime of a WSN by properly choosing a cluster head in a cluster, based on energy and pre-defined range. This reduces the energy consumption of nodes especially cluster heads in such a manner that redundancy is reduced and no overload takes place at CH.**

***Keywords*—WSN; LEACH; Clustering; Routing Protocol; Modified HETEROLEACH.**

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MCCS139

MODELING AND INVESTIGATION OF ELECTROTHERMALLY ACTUATED MICRO-GRIPPER

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***Abstract*— In the recent years, MEMS technology, because of its micro size has matured as a field of research. Micro-gripper is one of the applications of MEMS technology. This paper describes the design, simulation and analysis of micro-gripper based on electro-thermal actuator. An electro-thermally actuated micro-gripper has been designed, optimized and simulated using COMSOL Multiphysics simulation tool. The simulation of the gripper design is done by using copper as a structural material. Different parametric studies have been carried out such as displacement, stress and deformation by varying the driving voltage and temperature.**

Keywords — Microgripper, Finite Element Method (FEM), Meshing, Electro - thermal Actuators, MEMS, Joule Heating Principle, Thermal Expansion.

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MCCS141

AN ULTRA LOW POWER INTERNET CONTROLLED HOME AUTOMATION SYSTEM

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***Abstract*— In this paper an ultra-light low power and unique smart automation system has been implemented which interfaces the internet communication protocols like HTTP (Hyper Text Transfer Protocol) through an embedded Linux platform to obtain home automation. It has improved upon the pre-existing work by removing MOM type middleware, providing efficient M2M communication by implementing a direct virtual link between the transport layer of the two communicating devices.. This smart automation system is ultra-low powered and improves the efficiency and throughput involved in communication. An embedded Linux platform, connected to the internet through its Ethernet port, is used for the demonstration of this smart automation system. A web portal interface is used to give commands and receive updates about the result of automation.**

***Keywords*—Internet Of things (IoT), Embedded Linux Board, SSH Tunnelling, Home Automation System, Message-Oriented Middleware Architecture.**

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MCCS142

DEPTH AVERAGED VELOCITY DISTRIBUTION FOR SYMMETRICAL AND ASYMMETRICAL COMPOUND CHANNELS

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***Abstract*—Compound channels which consists of a main channel and its adjoining floodplains are very important for environmental, ecological, and design issues. The structures of the flow in such channels are rigorous because of the momentum transfer mechanism between the main channel and the floodplain. Flow mechanism in an asymmetrical compound channel is different than that of a symmetrical compound channel. There is a stronger interaction between the main channel flow and flood plain flow for an asymmetrical compound channel where as in symmetric compound channel the interaction is distributed from the both sides of the flood plain. Analysis of depth averaged velocity distribution in a compound channel is strongly influenced by the complex geometry associated with width ratio, aspect ratio and relative depth of both symmetric and asymmetric compound in channels. The variation of depth averaged velocity distribution in such channels for different geometry and flow conditions has been analysed. Proper prediction of depth averaged velocity distribution in a compound channel is depending upon the magnitude of shear layer for which the advanced soft ware CES is not providing accurate prediction especially for asymmetrical compound channel. Suggestions and improvements to predict depth averaged velocity distribution in both symmetrical and asymmetrical compound channels have been made.**

***Keywords*—Symmetrical compound channel, Asymmetrical compound channel, Momentum transfer, Interface , Floodplain, Main channel, Regression analysis, Width ratio, Relative depth.**

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MCCS143

APPLICATION OF LATERAL DISTRIBUTION METHOD AND MODIFIED-LATERAL DISTRIBUTION METHOD TO COMPOUND CHANNEL HAVING CONVERGING FLOODPLAIN

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***Abstract*— This paper examines the use of LDM (Lateral Distribution Method) and Modified-LDM in the computation of depth averaged velocity and boundary shear stress distribution of compound channel having converging flood plain. In overbank flow the main channel flow is affected by the floodplains and the conveyance capacity is usually reduced. The complexity of the problem rises more when dealing with a compound channel with non-prismatic floodplains. In non-prismatic compound channels with converging floodplains, due to change in floodplain geometry water flowing on the floodplain now crosses over water flowing in the main channel, resulting in increased interaction and momentum exchanges. This extra momentum exchange should also be taken into account in the flow modelling. In this research work the Modified LDM equation which consider friction slope and LDM equation is discretized by finite difference scheme and for solving those equations, MATLAB tool is used. Depth averaged velocity and boundary shear stress distribution obtained from LDM and MLDM is compared with the experimental dataset.**

***Keywords*—Depth averaged velocity, bounadary shear stress, LDM, Modified-LDM, MATLAB**

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MCCS151

DESIGN OF CMOS INTEGRATOR CIRCUIT FOR SIGMA DELTA ADC

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Abstract— In this research article Design of CMOS Integrator Circuit For Sigma Delta ADC has been proposed. It behaves as a low pass filter for input signal and high pass filter for quantization noise. Here the input and output is measured across the capacitor. This circuit is designed using Cadence Virtuoso UMC90nm CMOS technology. For the proper operation of the circuit power supply is used +1.3V to -1.3V. As the input square wave is applied, during the positive half cycle the voltage across capacitor increases from zero to the maximum peak value of applied voltage. During the negative half cycle, the capacitor starts to discharge and comes to zero. This process repeats for the remaining cycles and a triangular wave is obtained.

Keywords— CMOS (Complementary Metal Oxide Semiconductor), Op-amp, negative feedback, capacitor, resister, etc.

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MCCS152

A 0.533 DB NOISE FIGURE & 7 MILLWATT NARROWBAND LOW NOISE AMPLIFIER FOR GLOBAL POSITION SYSTEM APPLICATION

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Abstract— In this research article Low Noise Amplifier circuit is proposed. This circuit is most important block of receiver system. In Wireless Communication system LNA used in receiver front-end circuitry. It should be necessarily having high Gain and minimum noise figure for optimum performance.
This work is an attempt to develop the same without disturbing stability and linearity in the circuit. The proposed low Noise figure LNA contains single ended cascode topology including the input matching network and output matching network at input and output sides respectively so that minimum components are required when the circuit follows for LNA IC fabrication. The CMOS Low Noise amplifier is designed through Cadence spectre RF simulation in standard UMC 90nm CMOS process. It is designed for 1.575 GHz frequency which seeks its application in GPS receiver. The parameters like gain, input matching, output matching, reverse isolation and stability are examined by S-parameters. The noise figure, 1dB compression point IIP3 and power consumption are also examined for 1.5V input LNA. The proposed LNA is compared with existing LNA for performance analysis using the above parameters.

Keywords— Cascode transistor, Gain, Impedance Matching, Source Degenerated LNA, Global Positioning System (GPS).

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MCCS181

DESIGN OF ULTRA LOW POWER CMOS CLASS E POWER AMPLIFIER

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Abstract:– This paper is proposed to design an ultra-low CMOS class-E Power Amplifier (PAs) circuit to analyse its power gain and output power in PSS (periodic steady state response). A technique is presented to facilitate the control power of the RF PAs (radio frequency power amplifier).The basic circuit of RF PA is designed which has different switching actions as different values of capacitors are taken into account. A driver F stage is added in the basic circuit which increases the switching action considerably. When the voltage is high, current is low and when voltage is low, current is high, thus minimising the power dissipation. The PAE obtained is 78% and power gain is 60dB.

Keywords: CMOS (Complementary Metal Oxide Semiconductor), Power Amplifier, Power Added Efficiency, Power Gain.

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MCCSB102

CRYPTIC MINING FOR AUTOMATIC VARIABLE KEY BASED CRYPTOSYSTEM

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***Abstract*— This chapter introduces you to the basic concepts of Cryptic mining, a specialized data mining discipline for cryptic processing technique. This chapter explores the various tasks, models; and techniques that are used in cryptic mining in order to understand useful patterns and information from large and -unorganized captured cipher logs. It also provides examples and sample scenarios for readers to grasp the concepts at its first instance itself.**

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MCCSB105

NOC DESIGN FOR INTERCONNECTING MULTI-CORES

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***Abstract*— This chapter focuses on the design and implementation of an interconnection network for connecting multiple cores. The chapter begins with a discussion on the underlying principles involved in the design of a NoC (Network on Chip) delving into the different topologies, routing mechanisms, flow control mechanisms and router design. The state of art in multi-core interconnections is dealt with subsequently. A detailed insight in to a novel interconnection designed and implemented by the authors for improving the performance of scale-out workloads along with the simulation results is presented to enrich the reader's understanding of interconnection networks.**

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MCCSB106

SOME RECENT DIRECTIONS TOWARDS DESIGN OF AVK BASED SYMMETRIC CRYPTOSYSTEM

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***Abstract*— To enhance the security of symmetric key cryptosystem, large key size is desirable. But it may not be suitable for low power devices due to higher computation will be done for longer keys and that will demand for more power requirement and slow performance of device. Automatic Variable Key (AVK) can be an alternative with fixed length of key and it varies in every session. Further enhancement in level of security can be achieved by exchanging the parameters instead of keys between the communicating entities, These parameters will be used to generate session keys at the both end. This chapter presents schemes of the above specified Mechanism. Parameterized model has been demonstrated with various schemes and issues with analysis from cryptanalysis perspectives. This chapter also highlights the benefits of this model to ensure two level of security with characterization of methods for AVK and Estimation of key computation based on parameters only and finds application in low power device communication including components of Internet of Things(IOT).**

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MCCSB107

SILICON-GERMANIUM CHANNEL HETEROSTRUCTURE P-MOSFETS

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***Abstract*— Heteroepitaxy techniques for the growth of group IV binary alloys, in particular, SiGe films are reviewed. MBE perhaps offer the broadest range of growth conditions and mostly used as a research tool. UHVCVD offers the possibility of multiwafer growth, which is certainly attractive for volume production. For compatibility of the Si1-xGex/Si material system with the present Si processing technology, an important requirement is to realize high quality ultrathin dielectrics at a low temperature. The hole confinement in the SiGe well is demonstrated by simulation and from C-V characteristics. The design trade-off for SiGe channel p-MOSFET devices have been presented. The device behavior is studied using a 1-D Poisson Solver. The choice of gate material, optimization of the SiGe channel width and profile, Si cap and gate oxide thicknesses, the method of threshold voltage adjustment have been addressed.**

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MCCSB108

DIGITAL IC DESIGN &TECHNOLOGY

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***Abstract*— In this chapter we study the concept of digital hardware design & technology. This chapter deals the standard chips design, programmable logic devices, full-custom and semi-custom IC design, basic design loops, structure of computer and digital hardware design units. Implementation of technology: transistor switching, NMOS, CMOS logic gates, standard chips, MOS fabrication, noise margin, dynamic and static operation of logic gates, transmission gates, implementation of SPLD, CPLD & FPGAs.**