Winter School on

Digital System Design with Verilog

The ISVE with collaborative institutions are organizing **Winter School on Digital VLSI Design with Verilog** from 26-30th Dec 2024 in online mode.

Who can attend?: Students from EEE/ECE/CSE/IT 2nd year onwards are eligible for this course.

Course Information Details: https://isve.in/content/main/44

Registration Form (Send the filled scan copy of registration form to e-mail: isve.ranchi@gmail.com**):** https://www.isve.in/ContentUploaded/adminisve/files/Registration%20Form_Winter%20School-2024.pdf

Online Registration Link:

https://docs.google.com/forms/d/e/1FAIpQLSdPdHbecXEBD7f0R7PsRnXsoKbFpEfk4rOdyK-2LNWyNnPcvQ/viewform

About the Verilog: This is HDL (Hardware Description Language) used to model the electronic circuits and systems. It is most commonly used in the design and verification of digital circuits at the register -transfer level of the abstractions. It is most demanding course in electronics industry.

About the Experts: This course will be taught by Academia and Industry experts.

Course Timing: Course will run daily in evening 6:00pm onwards by which college students and industry professionals can attend easily. Course will cover theory with practical.

Advanced Course with Placement: Advanced course will also be offered after this course and interested can opt and register, who wish to make their carrier in VLSI Design/Chip Design and verifications.

Contact us: For any help and clarification try to contact via mail : isve.ranchi@gmail.com

Program Schedule for WS-DSDV-2024

Date	Name of Expert	Affiliations	Topic to be Covered
26.12.2024	**Dr. Vijay Nath**	VLSI Design Group, Department of ECE,BIT Mesra Ranchi	Fundamental of Digital System Design with Verilog
27.12.2024	**Dr. Vijay Nath**	VLSI Design Group, Department of ECE,BIT Mesra Ranchi	Combinational Circuit Design with Verilog
28.12.2024	**Dr. Khaleelu Rahman**	Department of ECE, CBIT Hyderabad	Combinational Circuit Implementation on FPGA
29.12.2024	**Dr. Adesh Kumar**	Dept. of ECE, UPES University Dehradun	Sequential Circuit Design
29.12.2024	**Dr. Vijay Nath**	VLSI Design Group, Department of ECE,BIT Mesra Ranchi	Sequential Circuit Design with Verilog
30.12.2024	**Sh. Shreyaskumar Patel**	Sr. Software Engineer NetScout Systems Inc, IEEE, Anna, Texas, USA	Verilog Based Embedded System Design
30.12.2024	**Dr. Khaleelu Rahman**	Department of ECE, CBIT Hyderabad	Sequential Circuit Implementation on FPGA