INDIAN SOCIETY FOR VLSI EDUCATION
RANCHI-835217 (JHARKHAND) INDIA
Matusri Engineering College, Hydradabad

Summer Internship-2025

Digital System Design with Verilog/ Digital System Design with VHDL/ Embedded System Design /FPGA based System Design/ Chip Design/ Microelectronics & VLSI Design

Inauguration of Program: 15.05.2025

Google Meet link for Joining: https://meet.google.com/gbo-irhy-zcs

Introduction of Summer Internship	**Dr. D.K. Yadav** President ISVE Ranchi/ Executive Committee Members	6:00pm-6:15pm
Message from Guest of Honor	**Dr Kavita Thakur** Professor, PRSU Raipur	6:16pm-6:40pm
Message from Zonal Mentor	**Dr. N. Srinivasa Rao** MEC Hyderabad	6:41pm-6:45pm
Message from Chief Guest	**Sh. K. K. Thakur** Former CGMT BSNL Jharkhand Circle Ranchi & Brand Ambassador of ISVE Ranchi	6:46pm-6:50pm

Summer Internship-2024 Zonal Coordinator Hyderabad (Telangana C AP)	**Dr. Nukala Srinivasa Rao** Professor C Head, ECE Matusri Engineering College Saidabad, Hyderabad
General Chair	**Dr. Vijay Nath** BIT Mesra (9973886214)
Coordinator	**Dr. Raj Kumar Singh** RU Ranchi
Organizing Secretary	**Dr. Anand Kumar Thakur** RU Ranchi
Convenor	**Dr. Kavita Thakur**, PRSU Raipur

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Moderator	**Mrs. T. Snehitha Reddy & Mrs. Nikhat Anjum**
For any query Contact at	isve.ranchi@gmail.com

Program Schedule

Duration of the Course	**15th May 2025**	**14th June 2025 & Further**
Timing for starting the courses (Monday to Friday)		**6:00pm**
Google Meet link for Joining: https://meet.google.com/gbo-irhy-zcs		

SN	Date	Name of Speaker	Topic of Internship
1	15.05.2025 (Thursday)	**Sh. Shreyaskumar Patel** NetScout Systems, USA	Embedded System Design
2	16.05.2025 (Friday)	**Dr. Adesh Kumar** UPES, UK	Digital System Design with VHDL
3	17.05.2025 (Saturday)to 18.05.2025 (Sunday)	Assignment Execution	
4	19.05.2025 (Monday)	**Dr. Vijay Nath** BIT Mesra	Digital System Design with Verilog
5	20.05.2025 (Tuesday)	**Sh. Shreyaskumar Patel** NetScout Systems, USA	Embedded System Design
6	21.05.2025 (Wednesday)	**Dr. Adesh Kumar** UPES, UK	Digital System Design with VHDL
7	22.05.2025 (Thursday)	**Dr. Vijay Nath** BIT Mesra	Digital System Design with Verilog

8	23.05.2025 (Friday)	**Sh. Shreyaskumar Patel** NetScout Systems, USA	Embedded System Design
9	24.05.2025 (Saturday) to 25.05.2025 (Sunday)	Assignment Execution	
10	26.05.2025 (Monday)	**Dr. Adesh Kumar** UPES, UK	Digital System Design with VHDL
11	27.05.2025 (Tuesday)	**Dr. Vijay Nath** BIT Mesra	Digital System Design with Verilog
12	28.05.2024 (Wednesday)	**Sh. Shreyaskumar Patel** NetScout Systems, USA	Embedded System Design
13	29.05.2025 (Thursday)	**Dr. Adesh Kumar** UPES, UK	Digital System Design with VHDL
14	30.05.2024 (Friday)	**Dr. Vijay Nath** BIT Mesra	Digital System Design with Verilog
15	31.05.2025 (Saturday) to 01.06.2025 (Sunday)	Assignment Execution	
16	02.06.2025 (Monday)	**Sh. Shreyaskumar Patel** NetScout Systems, USA	Embedded System Design
16	03.06.2025 (Tuesday)	**Dr. Adesh Kumar** UPES, UK	Digital System Design with VHDL
17	04.06.2025 (Wednesday)	**Dr. Vijay Nath** BIT Mesra	Digital System Design with Verilog
18	05.06.2025 (Thursday)	**Sh. Shreyaskumar Patel** NetScout Systems, USA	Embedded System Design
19	06.06.2025 (Friday)	**Dr. B. Khaleelu Rahman** (CBIT Hyderabad)	Digital System Design with VHDL
20	07.06.2025 (Saturday) to 08.06.2025 (Sunday)	Assignment Execution	

21	09.06.2025 (Monday)	**Dr. Vijay Nath** BIT Mesra	Digital System Design with Verilog
22	10.06.2025 (Tuesday)	**Sh. Shreyaskumar Patel** NetScout Systems, USA	Embedded System Design
23	11.06.2024 (Wednesday)	**Dr. Vijay Nath** BIT Mesra	Digital System Design with Verilog
24	12.06.2025 (Thursday)	**Dr. B. Khaleelu Rahman** (CBIT Hyderabad)	Digital System Design with VHDL
25	13.06.2025 (Friday)	**Simran Khokha** Infineon Technologies, Germany	Embedded System Design using Assembly Language/ Python
26	14.06.2025 (Saturday) to 15.06.2025 (Sunday)	Assignment Execution	
27	16.06.2025 (Monday)	**Sh. Shreyaskumar Patel** NetScout Systems, USA	Embedded System Design
28	17.06.2025 (Tuesday)	**Dr. Adesh Kumar** UPES, UK	Digital System Design with VHDL
29	18.06.2025 (Wednesday)	**Dr. Vijay Nath** BIT Mesra	Digital System Design with Verilog
30	19.06.2025 (Thursday)	**Simran Khokha** Infineon Technologies, Germany	Embedded System Design using Assembly Language/ Python
31	20.06.2025 (Friday)	**Vidushi Goel** Synopsis Pvt. Ltd.	Chip Design & Verification
32	21.06.2025 (Saturday) to (22.06.2025) (Sunday)	Assignment Execution	
33	23.06.2025 (Monday)	**Sh. Shreyaskumar Patel** NetScout Systems, USA	Embedded System Design
34	24.06.2025 (Tuesday)	**Dr. Adesh Kumar** UPES, UK	Digital System Design with VHDL

35	25.06.2025 (Wednesday)	**Dr. Vijay Nath** BIT Mesra	Digital System Design with Verilog
36	26.06.2025 (Thursday)	**Simran Khokha** Infineon Technologies, Germany	Embedded System Design using Assembly Language/ Python
37	27.06.2025 (Friday)	**Vidushi Goel** Synopsis Pvt. Ltd.	Chip Design & Verification
38	28.06.2025 (Saturday) to (29.06.2025) (Sunday)	Assignment Execution	
Further program will be executed accordingly, and the next schedule will be display			

ISVE Summer Internship-2025

Organizing Committee