



INDIAN SOCIETY FOR VLSI EDUCATION

RANCHI-835217 (JHARKHAND) INDIA

Matusri Engineering College, Hydradabad

Dr. D.Y. Patil Institute of Technology, Pimpri, Pune, Maharashtra



DYP DPU

Summer Internship Program-2025 Phase 2

Digital System Design with Verilog/ Digital System Design
with VHDL/ Embedded System Design / Chip Design/
Microelectronics & VLSI Design/ Data Science/ IoT/ Cyber
Security

Inauguration of Program: 25.07.2025

Google Meet link for Joining: <https://meet.google.com/gbo-irhy-zcs>

Introduction of Summer Internship	Dr. D.K. Yadav President ISVE Ranchi/ Executive Committee Members	6:00pm-6:15pm
Message from Guest of Honor	Dr Kavita Thakur Professor, PRSU Raipur	6:16pm-6:40pm
Message from Zonal Mentor	Dr. N. Srinivasa Rao MEC Hyderabad	6:41pm-6:45pm
Message from Chief Guest	Sh. K. K. Thakur Former CGMT BSNL Jharkhand Circle Ranchi & Brand Ambassador of ISVE Ranchi	6:46pm-6:50pm
Summer Internship-2025 Zonal Coordinator Hyderabad (Telangana C AP)	Dr. Nukala Srinivasa Rao Professor C Head, ECE Matusri Engineering College Saidabad, Hyderabad	
Summer Internship-2025 Zonal Coordinator Pimpri Pune (Maharashtra)	Dr. D.G. Bhalke Professor & Head, ETC, Dr. D.Y. Patil Institute of Technology, Pimpri, Pune	
General Chair	Dr. Vijay Nath BIT Mesra (9973886214)	
Coordinator	Dr. Raj Kumar Singh RU Ranchi	
Organizing Secretary	Dr. Anand Kumar Thakur RU Ranchi	



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Convenor	Dr. Kavita Thakur, PRSU Raipur
Moderator	Mrs. T. Snehitha Reddy & Mrs. Nikhat Anjum
For any query Contact at	isve.ranchi@gmail.com

Program Schedule

Duration of the Course	25 th July 2025	24 th August 2025 & Further	
Timing for starting the courses (Monday to Friday)	6:00pm		
Google Meet link for Joining: https://meet.google.com/gbo-irhy-zcs			
SN	Date	Name of Speaker	Topic of Internship
1.	25.07.2025 (Friday)	Dr. Adesh Kumar UPES, UK	Digital System Design with VHDL
2.	26.07.2025 (Saturday) & 27.07.2025 (Sunday)	Assignment Execution	
3.	28.07.2025 (Monday)	Dr Priyanka Srivastava SBU Ranchi	Embedded System Design/ Data Science
4.	30.07.2025 (Wednesday)	Dr. Vijay Nath BIT Mesra	Digital System Design with Verilog/ Microelectronics & VLSI Design
5.	01.08.2025 (Friday)	Dr. Adesh Kumar UPES, UK	Digital System Design with VHDL
6	02.08.2025 (Saturday)to 03.08.2025 (Sunday)	Assignment Execution	
7	04.08.2025 (Monday)	Dr. Vijay Nath BIT Mesra	Digital System Design with Verilog/ Microelectronics & VLSI Design



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8	06.08.2025 (Wednesday)	Dr Priyanka Srivastava SBU Ranchi	Embedded System Design/ Data Science
9	08.08.2025 (Friday)	Dr. Adesh Kumar UPES, UK	Digital System Design with VHDL
10.	09.08.2025 (Saturday) to 10.08.2025 (Sunday)	Assignment Execution	
11.	11.08.2025 (Monday)	Dr. Vijay Nath BIT Mesra	Digital System Design with Verilog/ Microelectronics & VLSI Design
12.	13.08.2025 (Wednesday)	Dr. Manoj Yadav Haryana	Embedded System Design/ Data Science
13.	15.08.2025 (Friday)	Dr. Khaleelu Rahman CBIT, Hyderabad	Digital System Design with VHDL
14.	16.08.2025 (Saturday) to 17.08.2025 (Sunday)	Assignment Execution	
15.	18.08.2025 (Monday)	Dr. Vijay Nath BIT Mesra	Digital System Design with Verilog
16.	20.08.2025 (Wednesday)	Dr. Adesh Kumar UPES, UK	Digital System Design with VHDL
17.	22.08.2024 (Friday)	Dr. Jeet Banerjee Adamas University, Kolkata	Embedded System Design/ Internet of Things/Cyber Security
18.	23.08.2025 (Saturday) to 24.08.2025 (Sunday)	Assignment Execution	
19.	25.08.2025 (Monday)	Dr. Vijay Nath BIT Mesra	Digital System Design / Microelectronics & VLSI Design



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20.	27.08.2025 (Wednesday)	Dr. Khaleelu Rahman CBIT, Hyderabad	Digital System Design with Verilog
21.	29.08.2025 (Friday)	Dr Priyanka Srivastava SBU Ranchi	Embedded System Design/ Data Science
22.	31.08.2025 (Saturday) to 01.09.2025 (Sunday)	Assignment Execution	
23.	02.09.2025 (Monday)	Dr. Vijay Nath BIT Mesra	Digital System Design with Verilog/ Microelectronics & VLSI Design
24.	04.09.2025 (Wednesday)	Dr. Adesh Kumar UPES, UK	Digital System Design with VHDL
25.	06.09.2025 (Friday)	Dr. Neeti Singh IMD, Delhi	Embedded System Design/ Data Science
26.	07.09.2025 (Saturday) to 08.09.2025 (Sunday)	Assignment Execution	
27.	10.09.2025 (Monday)	Dr. Vijay Nath BIT Mesra	Digital System Design with Verilog
28.	11.09.2025 (Wednesday)	Dr. B. Khaleelu Rahman (CBIT Hyderabad)	Digital System Design with VHDL
29.	13.09.2025 (Friday)	Sh. Shreyaskumar Patel NetScout Systems, USA	Embedded System Design
30	14.09.2025 (Saturday) to 15.09.2025 (Sunday)	Assignment Execution	

**ISVE Summer Internship Program-2025 /
ISVE Summer Training Program Phase 2
Organizing Committee**